REMARKS

These remarks are in response to the Office Action dated June 5, 2006 (Office Action). As this reply is timely filed, no fee is believed due. Claims 1, 11, and 21 have been amended to clarify various aspects of the present invention. Claims 9, 19, and 29 have been amended only to correct typographical errors. Claims 3, 13, and 23 have been cancelled. Accordingly, claims 4, 14, and 24 have been amended only to correct claim dependencies as these claims depended from now cancelled claims 3, 13, and 23, respectively. Support for these amendments can be found throughout the Applicants' specification and, more particularly, in paragraphs 24-33, 41, and FIGS. 2-5. No new matter has been introduced. Claims 1-2, 4-12, 14-22, and 24-30 are now pending.

In the Office Action, claims 1, 11, and 21 have been rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. The Office Action notes that with respect to the steps relating to "identifying a cost function" and "annealing the circuit design to determine a floorplan using the cost function", the cost function is not defined within the claims and the phrase "using a cost function" is ambiguous.

Claims 1, 11, and 21 have been amended to clarify the present invention. The step relating to "identifying a cost function" has been deleted. The step of "annealing the circuit design" has been amended to recite "annealing the circuit design to determine a floorplan by, at least in part, selecting a different shape from the set of shapes corresponding to at least one module and applying the selected shape to the at least one module, wherein each iteration of annealing the circuit design is evaluated according to evaluation of a cost function". In view of these amendments, withdrawal of the 35 U.S.C. § 112, second paragraph rejection of claims 1, 11, and 21 is respectfully requested.

Turning to the rejections on the art, claims 1-30 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,779,169 to Singh et al. (Singh). Singh discloses a method of positioning components on a target device.

Singh, however, fails to teach or suggest the Applicants' invention as recited in the claims.

With respect to claims 1, 11, and 21, the Office Action asserts that Singh discloses "determining a set of shapes associated with at least one module". In support, the Office Action notes that a "user may specify a size of [a] logic region". The Office Action further asserts that Singh teaches that the size of logic regions can be reshaped, citing FIG. 7. The Office Action goes on to suggest that since logic regions can be reshaped, a plurality of shapes can be determined.

The teachings of Singh, however, differ substantially from Applicants' invention as recited in the claims. At column 6, line 59 – column 7, line 6, Singh states:

> Notice that the locations of logic regions 901 and 902 cannot be swapped because they have different sizes. To make this move, the location of logic region 901 is extended outwards until it is the same size of logic region 902 as shown by dotted region 910. This extension also encapsulates the logic region 902 as shown by dotted region 920. The location of the extended region of the logic region 901, which also includes logic region 903, may now be swapped with the location of the logic region 902. The extension procedure of the third guideline is not always possible, however, as shown by the move denoted Swap 2. This swap attempts to move logic region 904 to the location occupied by 902. If the location of logic region 904 was extended to the size of 902 as shown by dotted region 930, it would intersect only a portion of the logic region 905.

In this passage, Singh teaches that to swap two regions, the regions must be of equal size. In some cases where the two regions to be swapped are not of equal size, the smaller region can be extended outward until it becomes the same size as the region with which it is to be swapped (target region). Clearly, the size to which a given region is to be extended cannot be known until the target region is ascertained. This occurs during annealing. Thus, the extension of a region is performed during annealing to "fit" that region, by extension, to the target region. Singh also is clear that regions simply are extended outward. Moreover, Singh explicitly states that the "extension procedure . . . is not always possible".

As amended, Applicants' claims 1, 11, and 21 recite "prior to annealing the circuit design, determining a set of shapes associated with each module". Contrary to the teachings of Singh, the Applicants' claims recite that the set of shapes is

determined prior to annealing of the circuit design. Shapes are not modified, as taught by Singh, during annealing. Further, claims 1, 11, and 21 recite that a set of shapes is determined for each module. While Singh may alter the size of one region to effectuate a swap with another region, this may include only a single shape change and not a "set of shapes". In any case, Singh clearly states that the extension procedure is not always possible. Indeed, the extension procedure disclosed by Singh may not be needed in a given swap operation where the two regions to be swapped are of equal size. It follows that some regions have no other shapes associated with them at all. Therefore, Singh does not teach or suggest "prior to annealing the circuit design, determining a set of shapes associated with each module" as recited by claims 1, 11, and 21.

The Office Action further asserts that Singh teaches the use of simulated annealing techniques to implement a placement method using the cost function and the set of shapes for at least one module. In support, column 7, lines 56-60 of the Singh specification have been cited. The cited passage states:

> According to an embodiment of the present invention, simulated annealing techniques are utilized to implement the placement method. Simulated annealing is a stochastic optimization technique for finding near-optimal solutions in high-dimensional spaces.

Singh does disclose that simulated annealing can be used to implement a placement method.

Claims 1, 11, and 21, as amended, recite "annealing the circuit design ... by, at least in part, selecting a different shape from the set of shapes corresponding to at least one module and applying the selected shape to the ... module". This feature is utterly lacking from the cited passage of Singh. As noted, Singh does not teach or suggest that a plurality of shapes for each module is determined prior to annealing. Without determining a plurality of shapes for each module, Singh cannot "select" a shape from the plurality of shapes that corresponds to a module. Rather, as needed, and only in some cases, Singh discloses that a module is extended so that the extended module is the same size as another module.

Column 5, lines 25-38 and 39-50 of Singh also have been cited for the proposition that Singh teaches the reshaping of regions. The cited passages refer to

the case where regions are to be sized using an automatic sizing method. It appears that the automatic sizing method taught by Singh occurs prior to annealing. That is, the initial size of a module can be automatically determined. Again, Singh fails to teach or suggest that a plurality of shapes is determined for each module prior to annealing or that shapes from the sets of shapes are selected and applied to corresponding modules during annealing as recited in claims 1, 11, and 21.

With regard to claims 9, 19, and 29, it is asserted that Singh teaches that "each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed module to be placed within that module. In support, the Office Action notes that Singh teaches that logic elements (LE's) can be combined to form a logic-array block (LAB), and that LAB's can be combined to form a MegaLab.

Applicants have corrected typographical errors in claims 9, 19, and 29, which now recite "relatively placed macros" and not "relatively placed modules". The structures noted in Singh are different from relatively placed macros. LE's, LAB's, and MegaLab's refer to nothing more than the generic hierarchy of physical structures that form the target device, i.e., in terms of rows, columns, or the like. These structures and hierarchies are independent of any circuit design to be applied to the target device. A relatively placed macro indicates predetermined, relative coordinates of primitives in relation to one another. In any case, the Applicants' note that column 4, line 24 – column 5, line 12 teaches only that the size of regions is dependent upon n_{LE}, which refers to the number of LE's assigned to a logic region. Singh does not teach or suggest that "each shape of a set of shapes associated with a module has a minimum width and height of at least a width and height of a largest relatively placed macro to be placed within that module".

Applicants believe all remaining claims to be allowably on their own merits and by virtue of their dependence upon claims 1, 11, or 21.

As Singh fails to teach or suggest the features recited in Applicants' claims, withdrawal of the 35 U.S.C. § 102(e) rejection with respect to claims 1-12, 14-22, and 24-30 is respectfully requested. Applicant believes all claims to be in condition for allowance, which action is respectfully requested. The Applicant invites the Examiner

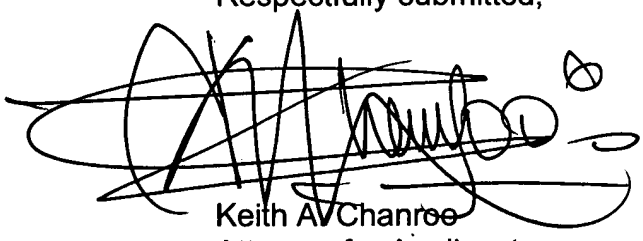
to call the undersigned if it is believed that a telephonic interview would expedite prosecution of the application to an allowance.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 23, 2006

Pat Tompkins — *Name*

Pat Tompkins — *Signature*